MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2016/2017

TAO1221 – COMPUTER ARCHITECTURE AND ORGANIZATION

(All sections / Groups)

01 MARCH 2017
9.00 a.m. – 11.00 a.m.
(2 hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 5 pages including cover page with 5 Questions only.

2. Attempt **ALL FIVE** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

QUESTION 1

(a) The ENIAC (Electronic Numerical Integrator and Computer), designed and constructed at the University of Pennsylvania, was the world's first general purpose electronic digital computer. Describe **SIX (6)** features of ENIAC. [3 marks]

(b) Identify the technology that is used for a computer from First Generation until Fourth Generation. [4 marks]

(c) Describe the benefits of the technology (in [b] above), that is used in Second Generation until Fourth Generation. [3 marks]

QUESTION 2

(a) Contemporary computer designs are based on concepts developed by John von Neumann at the Institute for Advanced Studies, Princeton. Describe **THREE (3)** principles of *von Neumann architecture*. [3 marks]

(b) Interrupt could improve the performance of a microprocessor. Discuss **TWO (2)** ways a microprocessor in handling multiple interrupts. [4 marks]

(c) List **THREE (3)** major components in a computer. Explain the functions of each component. [3 marks]

Continued ....

QUESTION 3

(a) Assume that **8-bit Two's Complement Scheme** is used for representing integers in one microprocessor.

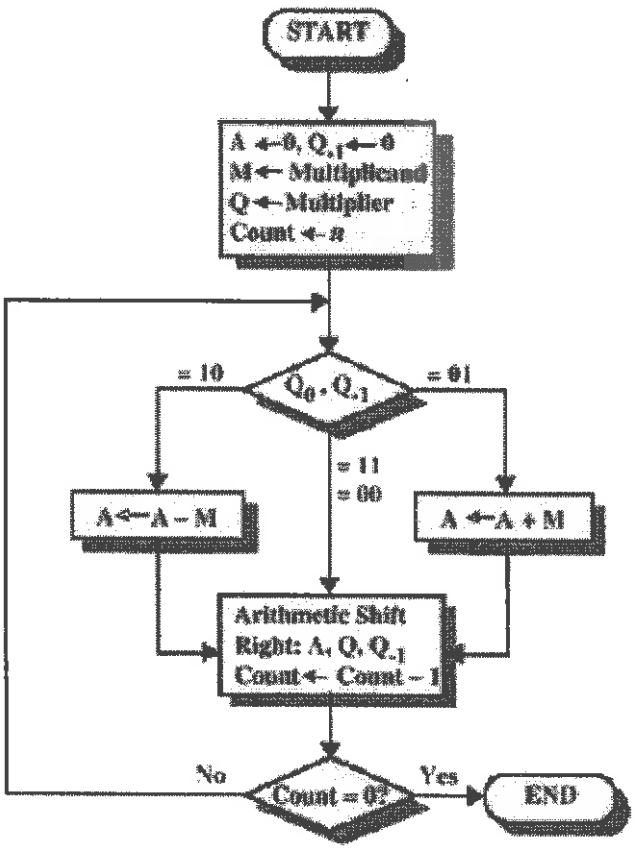
i. Represent the following decimal numbers in **8-bit Two's Complement Scheme**.

A = (27), B = (-107), C = (-84) [3 marks]

ii. Perform the following arithmetic operations using **8-bit Two's Complement Scheme**.

1. [A + B] [1 mark]
2. [C – A] [1 mark]

(b) Given the flowchart for Booth's Algorithm:



Show the steps using Booth's Algorithm in performing the multiplication of two **4-bit two's complement** binary numbers as given below:

Multiplicand (M) = $(0110)_2$ or $(6)_{10}$
Multiplier (Q) = $(1100)_2$ or $(-4)_{10}$

[5 marks]

Continued ....

QUESTION 4

(a) Write **ONE (1)** assembly language instruction for microprocessor Intel 8085 for each of the following action (refer to appendix for the 8085 instruction set):

i. Directly loads register C with a single byte of data 45H.
ii. Transfers data from register D to register B.
iii. Stores the content of the Accumulator into memory location 3457H.
iv. Adds 36H to the content of the accumulator.
v. Performs an Exclusive-OR operation bit by bit between the content of the Accumulator and the register C.

[5 marks]

(b) In 8085 microprocessor, explain the meaning of the following flags:

i. **Sign Flag** [1 mark]
ii. **Zero Flag** [1 mark]

(c) In 8085 microprocessor, assume that register A contains a word: 1011 0001. Specify the output of register A after each the following instruction is executed:

i. **RLC** (Rotate Accumulator left) [1 mark]
ii. **RRC** (Rotate Accumulator right) [1 mark]
iii. **RAR** (Rotate Accumulator right through Carry) with initial Carry=0 [1 mark]

QUESTION 5

(a) List **FOUR (4)** methods of accessing data in memory. Explain each of them. [4 marks]

(b) Compare between **Static RAM (SRAM)** and **Dynamic RAM (DRAM)** in terms of volatility, speed and usage. [3 marks]

(c) Describe **THREE (3)** advantages of using a multiprocessor over uniprocessor organizations. [3 marks]

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APPENDIX

8085 INSTRUCTION SET

INSTRUCTION SUMMARY

DATA TRANSFER INSTRUCTIONS

MOV	Copy from source to destination
MVI	Move immediate 8-bit
LDA	Load accumulator
LDAX	Load accumulator indirect
LXI	Load register pair immediate
LHLD	Load H and L registers direct
STA	Store accumulator direct
STAX	Store accumulator indirect
SHLD	Store H and L registers direct
XCHG	Exchange H and L with D and E
SPHL	Copy H and L registers to the stack pointer
XTHL	Exchange H and L with top of stack
PUSH	Push register pair onto stack
POP	Pop of stack to register pair
OUT	Output data from accumulator to a port with 8-bit address
IN	Input data to accumulator from a port with 8-bit address

ARITHMETIC INSTRUCTIONS

ADD	Add register or memory to accumulator
ADC	Add register to accumulator with carry
ADI	Add immediate to accumulator
ACI	Add immediate to accumulator with carry
DAD	Add register pair to H and L registers
SUB	Subtract register or memory from accumulator
SBB	Subtract source and borrow from accumulator
SUI	Subtract immediate from accumulator
SBI	Subtract immediate from accumulator with borrow
INR	Increment register or memory by 1
INX	Increment register pair by 1
DCR	Decrement register or memory by 1
DCX	Decrement register pair by 1
DAA	Decimal adjust accumulator

LOGICAL INSTRUCTIONS

CMP	Compare register or memory with accumulator
CPI	Compare immediate with accumulator
ANA	Logical AND register or memory with accumulator
ANI	Logical AND immediate with accumulator
XRA	Exclusive OR register or memory with accumulator
XRI	Exclusive OR immediate with accumulator
ORA	Logical OR register or memory with accumulator
ORI	Logical OR immediate with accumulator
RLC	Rotate accumulator left
RRC	Rotate accumulator right
RAL	Rotate accumulator left through carry
RAR	Rotate accumulator right through carry
CMA	Complement accumulator
CMC	Complement carry
STC	Set carry

BRANCHING INSTRUCTIONS

JMP	Jump unconditionally
JC	Jump on carry
JNC	Jump on no carry
JP	Jump on positive
JM	Jump on minus
JZ	Jump on zero
JNZ	Jump on no zero
JPE	Jump on parity even
JPO	Jump on parity odd
CALL	Call unconditionally
CC	Call on carry
CNC	Call on no carry
CP	Call on positive
CM	Call on minus
CZ	Call on zero
CNZ	Call on no zero
CPE	Call on parity even
CPO	Call on parity odd
RET	Return unconditionally
RC	Return on carry
RNC	Return on no carry
RP	Return on positive
RM	Return on minus
RZ	Return on zero
RNZ	Return on no zero
RPE	Return on parity even
RPO	Return on parity odd
PCHL	Load program counter with HL contents
RST	Restart

CONTROL INSTRUCTIONS

NOP	No operation
HLT	Halt
DI	Disable interrupts
EI	Enable interrupts
RIM	Read interrupt mask
SIM	Set interrupt mask

End of Paper.